REMARKS

Reconsideration of the pending application is respectfully requested on the basis of the following particulars:

1. Amendments and Support for Same

By the Response, claim 4 has been amended to further clarify the claimed features and to more particularly point out and distinctly claim the subject matter of the invention. No new matter has been added. Support for the amended features will be discussed in detail in response to the prior art rejections below. Accordingly, claims 4-9 are respectfully submitted for consideration. Approval and entry of the amendments are respectfully requested.

2. Rejections under 35 U.S.C. §103(a)

With respect to the rejection of claims 4-7 under 35 U.S.C. §103(a) as being unpatentable over Wright (US 6,467,042) in view of Dean (US 6,434,704), and with respect to the rejection of claims 8-9 under 35 U.S.C. §103(a) as being unpatentable over Wright and in view further of Dehghan (US 6,275,087), Applicant respectfully traverses the rejection at least for the reason that Wright, Dean, and Dehghan, combined or separately, fail to teach, disclose, or suggest all of the limitation recited in the rejected claims.

As amended, claim 4 recites an interface circuit including a detection portion which monitors the control signal to output a detection signal when there is a level change of the control signal, a process control portion which generates and switches an operation-enable signal and operation disable signal each time the detection signal is supplied thereto, a gated-clock oscillator which generates a gated clock signal for data transmission only when the operation-enable signal from the process control portion is supplied thereto, and a transmission function which performs the serial data transmission on the basis of the gated clock signal.

The Examiner contends that Wright describes Applicant's claimed feature of "a detection portion which monitors the control signal to output a detection signal when there is

a change in the control signal" in Fig. 2 and col. 3, lines 21-29. In response, Applicant has amended claim 4, as shown above, to further distinguish the claimed features over Wright.

Applicant respectfully asserts that Wright generally describes a traffic detect circuit 102 (i.e., TRAFFIC DETECT in Fig. 2 of Wright), which detects data traffic or non-idle state, as described in col. 3, lines 26-27 of Wright. However, Wright does not teach, disclose, or suggest that the traffic detect circuit being capable of detecting a level of change of a control signal, as recited in Applicant's amended claim 4.

Further, the Examiner contends in page 3, lines 1-3 of the Office Action that Wright describes "an oscillator circuit which generated a clock signal..." in Figs. 2 and col. 3, lines 30-35 and col. 4, lines 14-19 of Wright. However, Applicant respectfully submits that claim 4 actually claims "a gated-clock oscillator which generates a gated clock signal for data transmission only when the operation-enable signal from the process control portion is supplied thereto", which is not similar structurally and functionally to Wright's oscillator circuit 106 for the reasons set forth below.

According to Applicant's interface circuit, the detection portion (i.e., edge detection circuit 90b) detects a level change (i.e., "H" to "L", and vice versa) of the signal VBUS, and the process control portion generates an operation-enable signal ENB. The Examiner is invited to review page 15, line 25 to page 16, line 17 and signals VBUS and ENB at timing T2 and T3 in Fig. 4 of the specification for support of the claimed features.

Moreover, as recited in amended claim 4, the transmission function portion performs the serial data transmission on the basis of the gated clock signal, wherein the gated clock signal is generated responsive to the operation-enable signal ENB (i.e., the level change of the control signal). Thus, according to the embodiment recited in amended claim 4, a low-frequency clock signal (CLK) oscillation is unnecessary. Additionally, the interface circuit of the presently claimed invention has a configuration in which the power consumption is advantageously reduced when data transmission is not performed.

With respect to Dean and Dehghan, Applicant respectfully asserts that Dean and Dehghan also fail to teach, disclose, or suggest the above-discussed features that are deficient in Wright.

The requirements for establishing a *prima facie* case of obviousness, as detailed in MPEP § 2143 - 2143.03 (pages 2100-122 - 2100-136), are: first, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference to combine the teachings;

second, there must be a reasonable expectation of success; and, finally, the prior art reference (or references when combined) must teach or suggest all of the claim limitations.

Further, according to MPEP §2141(I), Patent examiners carry the responsibility of making sure that the standard of patentability enunciated by the Supreme Court and by the Congress is applied in each and every case. The Supreme Court in *Graham v. John Deere*, 383 U.S. 1, 148 USPQ 459 (1966), stated:

> Under § 103, the scope and content of the prior art are to be determined; differences between the prior art and the claims at issue are to be ascertained; and the level of ordinary skill in the pertinent art resolved. Against this background, the obviousness or nonobviousness of the subject matter is determined. Such secondary considerations as commercial success, long felt but unsolved needs, failure of others, etc., might be utilized to give light to the circumstances surrounding the origin of the subject matter sought to be patented.

Moreover, according to MPEP §2141(II), when applying 35 U.S.C. §103, the following tenets of patent law must be adhered to:

> (A) The claimed invention must be considered as a whole;
>
> (B) The references must be considered as a whole and must suggest the desirability and thus the obviousness of making the combination;
>
> (C) The references must be viewed without the benefit of impermissible hindsight vision afforded by the claimed invention; and
>
> (D) Reasonable expectation of success is the standard with which obviousness is determined.

In view of the amendment and arguments set forth above, Applicant respectfully requests the Examiner to follow tenets A-D in relying on Wright, Dean, and Dehghan. Further, Applicant respectfully requests reconsideration and withdrawal of the §103(a) rejection of claims 4-9 over Wright, Dean, and Dehghan.

3. Conclusion

In view of the foregoing amendments, it is respectfully submitted that the application is in condition for allowance. Accordingly, it is requested that claims 4-9 be allowed and the application be passed to issue.

If any issues remain that may be resolved by a telephone or facsimile communication with the Applicant's representative, the Examiner is invited to contact the undersigned at the numbers shown.

Further, while no fees are believed to be due, the Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 50-4525.

Respectfully submitted,

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